TELECOMMUNICATIONS RECEIVER WITH AUTOMATIC GAIN CONTROL

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001]   Not Applicable

STATEMENT OF FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[0002]   Not Applicable

5   ## BACKGROUND OF THE INVENTION

1.   TECHNICAL FIELD

[0003]   This invention relates in general to telecommunications and, more particularly, to a telecommunications receiver with automatic gain control.

2.   DESCRIPTION OF THE RELATED ART

10   [0004]   In a radio frequency receiver, an automatic gain control circuit is often used to compensate for variations in signal strength of the received signal. Variations in the signal strength of the received signal can occur for various reasons, such as changes in transmission distances, atmospheric conditions, changes in channels, obstructions in the transmission path, and so on.

15   [0005]   Accordingly, automatic gain control circuits are used to maintain a relatively stable output signal volume, despite varying input signal strength. Current solutions base gain adjustment decisions on a signal level measurement performed in a digital signal processor (DSP) after digital channel filtering has

been applied to the input signal. As a result, saturation may occur in the analog-to-digital converter (ADC) which translates the input signal (where the signal may be the superposition of the useful signal, DC offset, adjacent channels and blockers) to a digital signal for processing by the DSP. When saturation occurs,

5   signal information is irretrievably lost.

[0006]   Therefore, a need has arisen for a radio receiver with automatic gain control that avoids ADC saturation.

BRIEF SUMMARY OF THE INVENTION

[0007] In the present invention, a receiver comprises analog-to-digital circuitry for generating a digital representation of a signal at an input and adjustable gain control circuitry for receiving a radio signal and outputting an

5 amplified analog signal using a gain determined by a magnitude of the signal at the input of the analog-to-digital circuitry. Digital channel filtering circuitry filters the digital representation and digital processing circuitry processes the output of the digital representation.

[0008] The present invention provides significant advantages over the prior

10 art. By initiating gain changes in the automatic gain control circuit responsive to the signal at the input of the analog-to-digital circuit (where the signal may be the superposition of the useful signal, DC offset, adjacent channels and blockers), the gain control implementation permits optimal use of the analog-to-digital converter's dynamic range. The present invention allows reductions in gain only

15 when necessary, with subsequent optimization of receiver sensitivity.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0009]   For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

5   [0010]   Figure 1 illustrates a basic block diagram of a prior art digital radio receiver;

[0011]   Figure 2 illustrates a block diagram of a receiver with gain variations based on the magnitude of the signal converted by an analog-to-digital converter; and

10   [0012]   Figure 3 illustrates a state diagram showing an example of how the most significant bits of the output of the analog-to-digital converter can be used for gain control.

DETAILED DESCRIPTION OF THE INVENTION

[0013]   The present invention is best understood in relation to Figures 1 - 3 of the drawings, like numerals being used for like elements of the various drawings.

5   [0014]   Figure 1 illustrates a basic block diagram of a prior art digital radio receiver 10. An input signal is received on antenna 12, passed through bandpass filter 13, and amplified by amplifier 14. The amplified input signal is separated into I and Q components through mixers 16, which are coupled to carrier frequency signals, offset by 90 degrees. Both I and Q signals are subjected to

10   respective low pass filters 18. The outputs of low pass filters 18 are input to automatic gain control (AGC) circuits 20, which are set to the same gain. The output of the AGC circuits 20 are input to ADC circuits 22, which convert the signal to a binary representation. The outputs of the ADC's are coupled to digital channel filters 24. The output of the digital channel filters are coupled to a

15   processor 26, shown in Figure 1 as a digital signal processor (DSP).

[0015]   In operation, the output of one of the digital channel filters 24 is sampled by the DSP 26. If the signal level at the output of one of the digital channel filter 24 is too high, the AGC 20 is adjusted by the DSP 26 to reduce the level of the signal input to the ADC to avoid saturation. The AGC gain is set to

20   maintain a useful signal-to-noise ratio, referencing the useful signal to the noise floor.

[0016]   The circuit of Figure 1 may produce incorrect results in certain situations, because it measures the filtered signal being input to the DSP. Using GPRS (General Packet Radio Service), for example, either sensitivity or

25   interference tests may be used to set the automatic gain control. A sensitivity test determines whether a mobile device can successfully receive a signal at a very low level at the antenna 12. In this test, the receiving device is set to maximum

gain in order to minimize the receiver noise figure (i.e., to achieve the maximum signal-to-noise level at the input of the ADC 20). In the sensitivity test, since the received signal is very low, there is no chance of ADC saturation.

[0017]   In an interference test, however, an interferer is added to the useful

5   signal at the antenna. The useful signal is applied at the antenna at a level 20 dB above the sensitivity level. The interferer is applied at a high level; for instance, the interferer may be 41 dB above the useful signal in 2nd adjacent interference. When the receiver is at maximum gain, the interfering signal can make the ADC clip.

10   [0018]   As noted above, in GPRS, either a sensitivity test or an interference test may be used in the automatic gain strategy. The receiving device will not know which test is being used. Therefore, the receiver will set the gain to its maximum gain. Since the digital channel filter 24 will filter out the interfering signal, the signal applied to the DSP may remain within an acceptable range, although the

15   signal at the input of the ADC 22 may cause the ADC 22 to be at saturation or close to saturation. Accordingly, the gain will be set too high, resulting in a distorted signal.

[0019]   Figure 2 illustrates a block diagram of a receiver 30 which alleviates the problem set forth above. As in Figure 1, an input signal is received on

20   antenna 12, passed through bandpass filter 13, and amplified by amplifier 14. The amplified input signal is separated into I and Q components through mixers 16, which are coupled to carrier frequency signals, offset by 90 degrees. Both I and Q signals are subjected to respective low pass filters 18. The outputs of low pass filters 18 are input to automatic gain control (AGC) circuits 32, which are set

25   to the same gain. The output of the AGC circuits 32 are input to ADC circuits 22, which convert the signal to a binary representation. The outputs of the ADCs are coupled to respective digital channel filters 24. The output of the digital channel

filters are coupled to processor 26. The output of at least one ADC 22 is also coupled to an AGC 32.

[0020] In operation, the AGCs 32 adjust gain responsive to the magnitude of the signal input to one of the ADCs 22, prior to filtering by the digital channel

5   filter 24. The magnitude of the input signal to the ADC 22 may be determined using a set of most significant bits of the ADC output. Depending upon the urgency of the gain adjustment (i.e., depending upon how close the ADC is to saturation), the gain adjustment may be made directly by the AGC 32 without DSP intervention. For example, the gain may be reduced automatically by the

10   AGC 32 whenever the most significant bit of the ADC output is set to "1" and may be reduced or increased responsive to control signal from the DSP in other circumstances.

[0021] The output of the ADC 22 is thus used to determine the correct gain, rather than using the output of the digital channel filter 24 to determine the

15   correct gain. If the output of ADC exceeds a certain level, the gain can be adjusted downward to avoid clipping of the signal. Thus, if a sensitivity test is used, the low-power useful signal will not cause clipping and the gain can be set to its maximum. On the other hand, if an interference test is used, if the power of the two signals exceeds a certain level, the gain can be reduced, while

20   maintaining an adequate margin between quantification noise and useful signal at the ADC input, thus allowing more room for the interfering signal in the dynamic range of the ADC 22.

[0022] In the preferred embodiment, the gain adjustment is controlled by using a predetermined number of the MSBs (most significant bits) of the output

25   of one of the ADCs 22.

[0023] Figure 3 illustrates a state diagram showing an example of how the MSBs of the output of the ADC 22 can be used for gain control. This example

uses the three most significant output bits of one of the ADCs 22; however, more or less of the MSBs could be used in an actual implementation. Using more MSBs could provide greater resolution in the gain control, although with slightly more complexity.

5   **[0024]**   In state 40, the gain is held steady. While the three MSBs = "000", the gain is increased in state 42, potentially all the way to maximum gain (as would occur during the sensitivity test). Once the MSBs = "001" the gain is held steady in state 40.

[0025]   If MSBs = "01x" (where "x" indicates a don't care), the digital
10   baseband (i.e., the DSP 26) reduces the gain of the AGC by 6 dB. The gain would be repeatedly reduced by 6 dB until the MSBs return to "00x".

[0026]   If the MSBs = "1xx", then the gain is reduced by 20 dB, in order to avoid an immediate saturation problem at the ADC 22. In the preferred embodiment, the emergency gain reduction is performed without DBB
15   interaction; the DBB is informed by the AGC that the gain has been reduced. In the interfering channel test condition, the gain can be reduced by 20 dB without any performance degradation.

[0027]   In order to prevent hysteresis (oscillations between increasing gain and decreasing gain), the decision threshold between gain increase and gain decrease
20   should be different.

[0028]   While Figure 3 illustrates an embodiment for controlling gain, the thresholds for initiating a gain switch, and the magnitude of a given change, could be varied as desired.

[0029]   The present invention provides significant advantages over the prior
25   art. By initiating gain changes in the AGC responsive to the signal at the input of the ADC (where the signal may be the superposition of the useful signal, DC

offset, adjacent channels and blockers) the AGC implementation permits optimal use of the ADC's dynamic range. The degree of gain change may also be varied depending upon the magnitude of the signal at the input of the ADC. Gain control is thus compatible with GPRS test modes. If the ADC is integrated in the

5   RF chip, the detection is free, since the ADC can be used as the detector with the MSB bits of the output digital word indicating how far the ADC is from saturation.

[0030]   While a reduction in the receiver gain increases the noise floor, the present invention reduces gain only when necessary, with subsequent

10 optimization of receiver sensitivity. Whereas saturation completely removes information from the signal, a reduction of the signal-to-noise ratio will allow demodulation, with some BER (bit error rate) degradation.

[0031]   Although the Detailed Description of the invention has been directed to certain exemplary embodiments, various modifications of these embodiments,

15 as well as alternative embodiments, will be suggested to those skilled in the art. The invention encompasses any modifications or alternative embodiments that fall within the scope of the Claims.